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(54) **Storing video frame data in a memory**

(57) Video frame date in eg a MPEG decoder is divided into a first part and second part; the first part is stored in a first region of the memory, and the second part is stored in a second region of the memory while the stored first part is read from the memory; the second part is subsequently read from the memory. The second part may be read more than once to change the frame rate. A video frame may be divided into n-parts, a memory capable of storing 1/n of a frame being used.

FIG.4

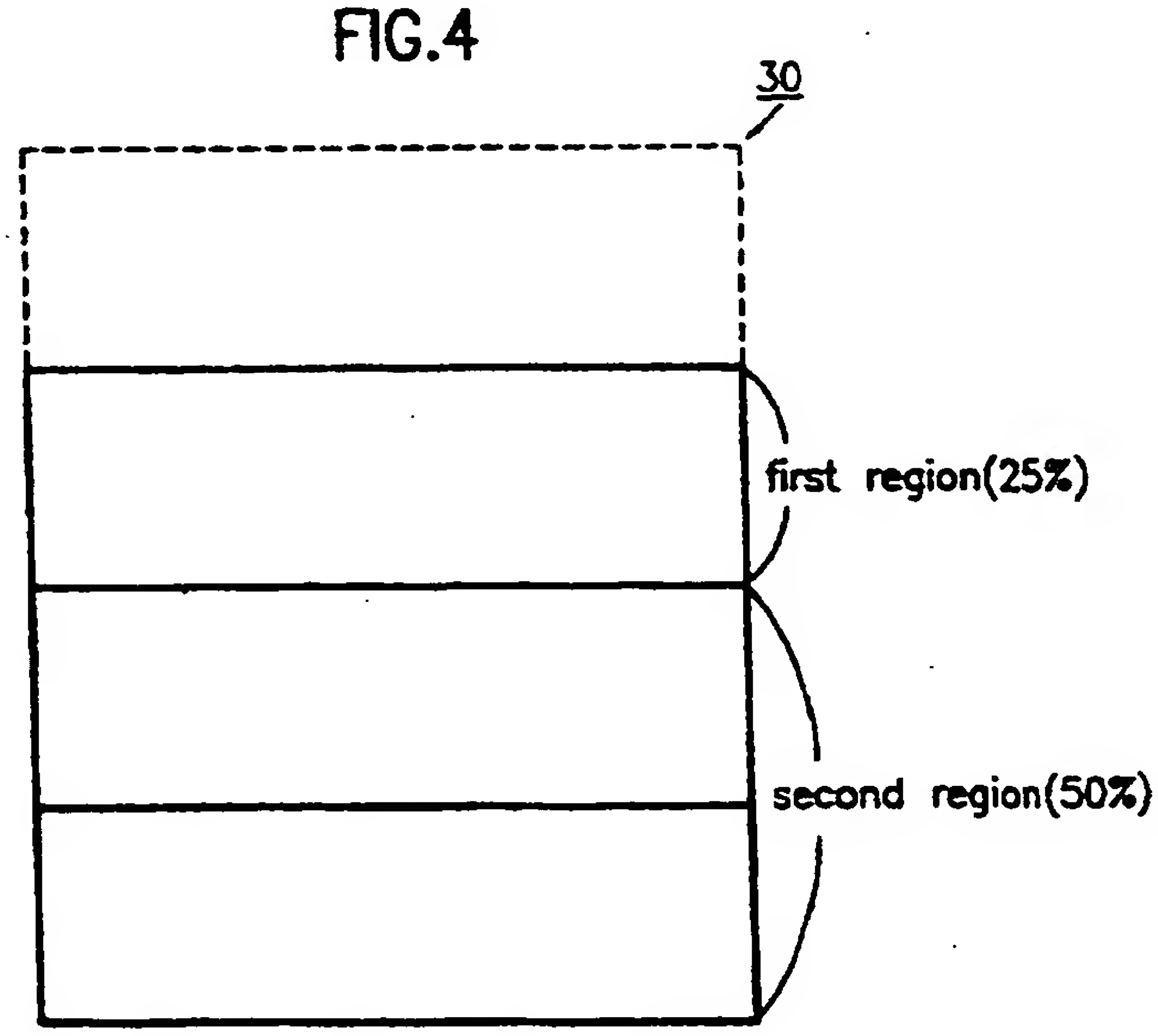

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FIG. 1a
prior art

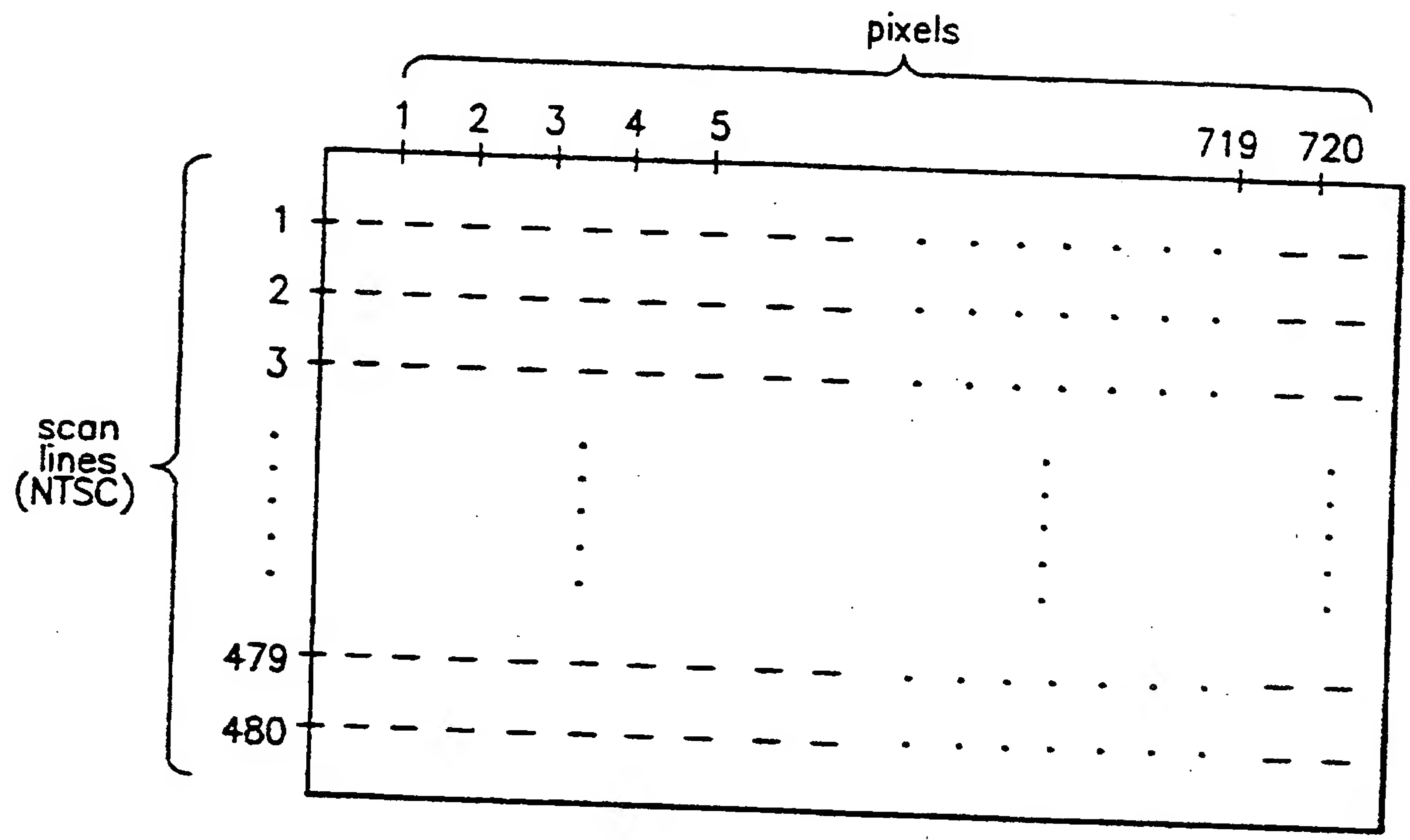


FIG. 1b
prior art

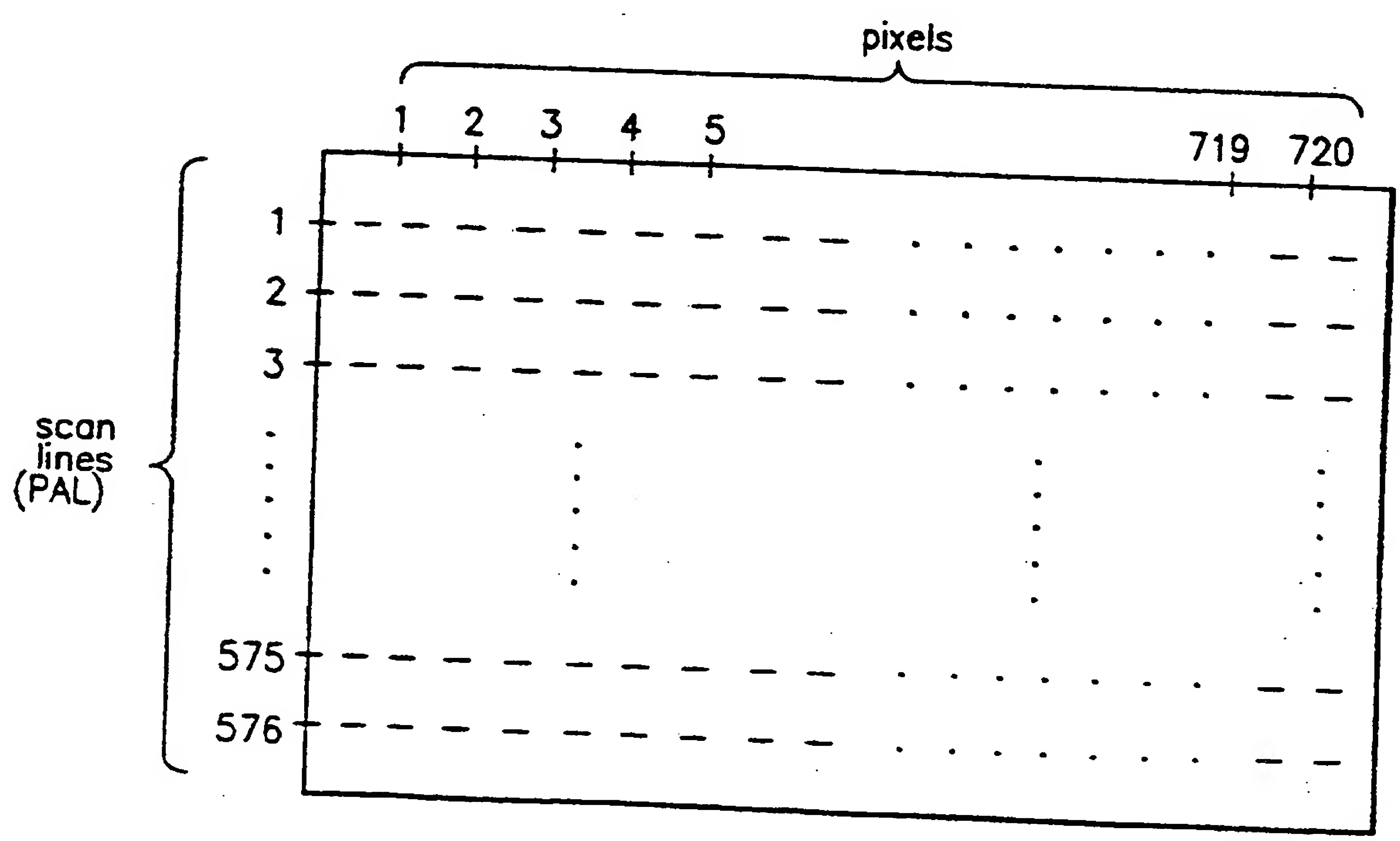


FIG.2

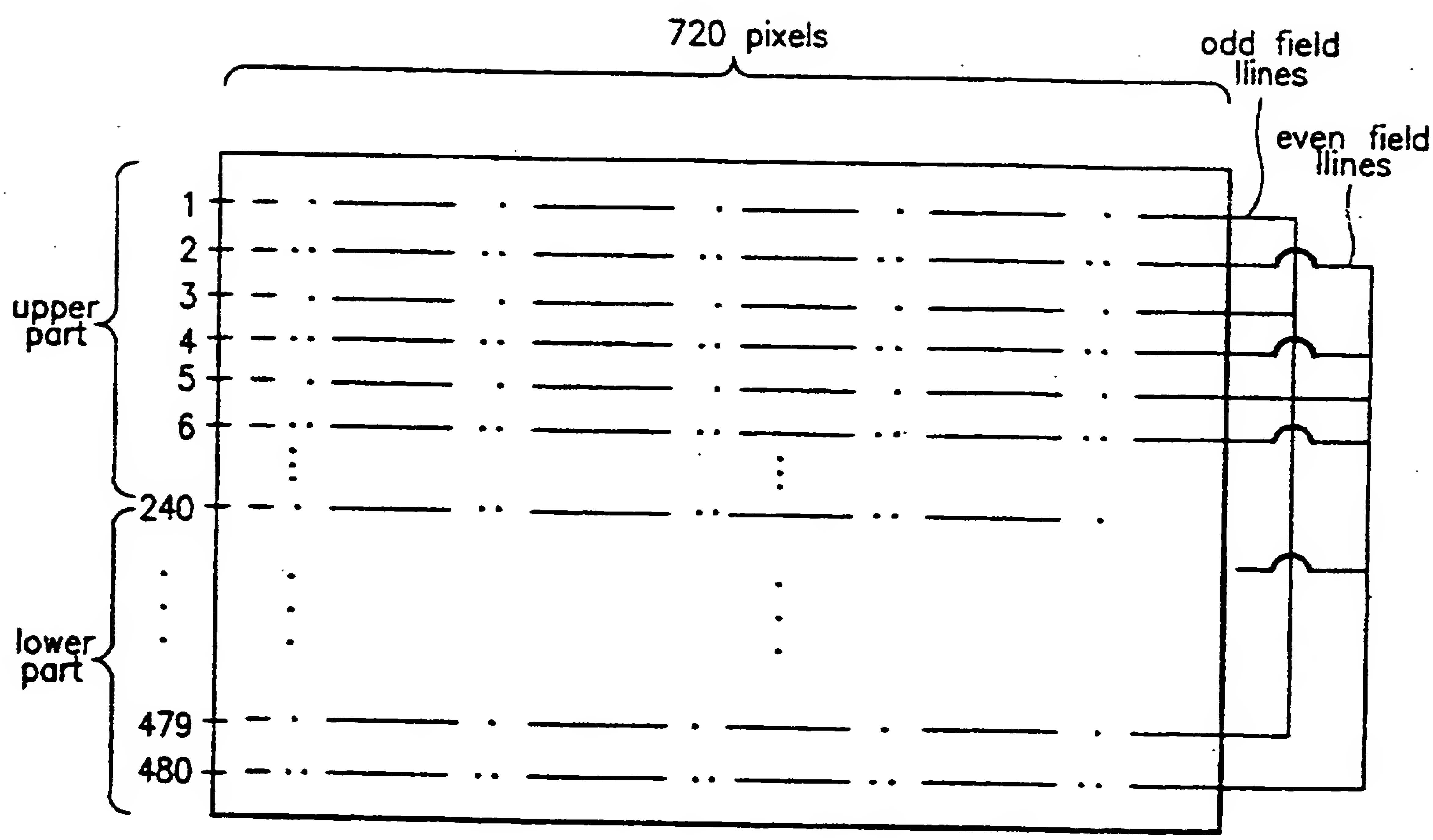

720 pixels
odd field llines
even field llines
upper part
lower part
1
2
3
4
5
6
240
479
480

FIG.3a

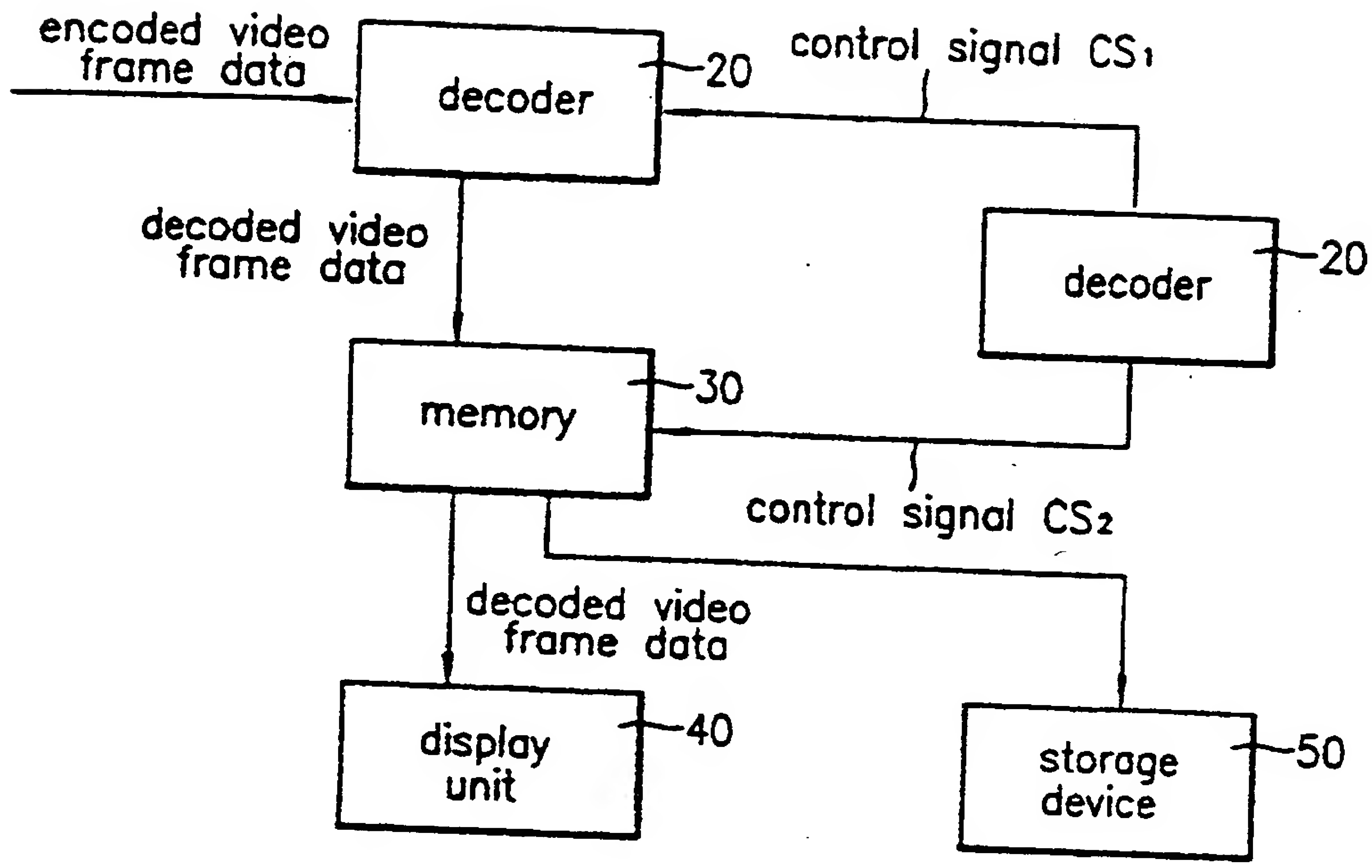

encoded video frame data
decoder
20
control signal CS1
decoder
20
decoded video frame data
memory
30
control signal CS2
decoded video frame data
display unit
40
storage device
50

FIG.3b

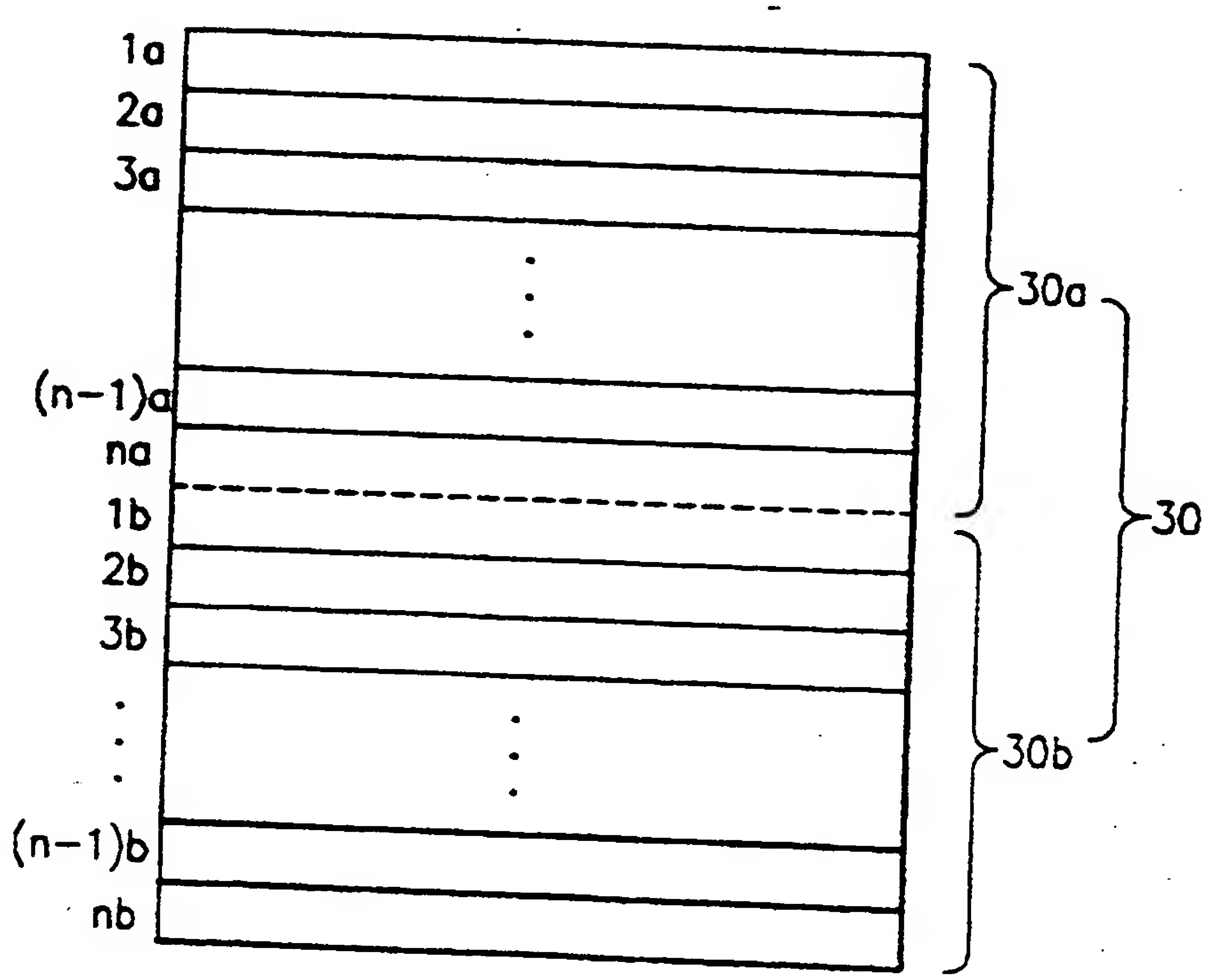

1a
2a
3a
(n-1)a
na
1b
2b
3b
(n-1)b
nb
30a
30
30b

FIG.4

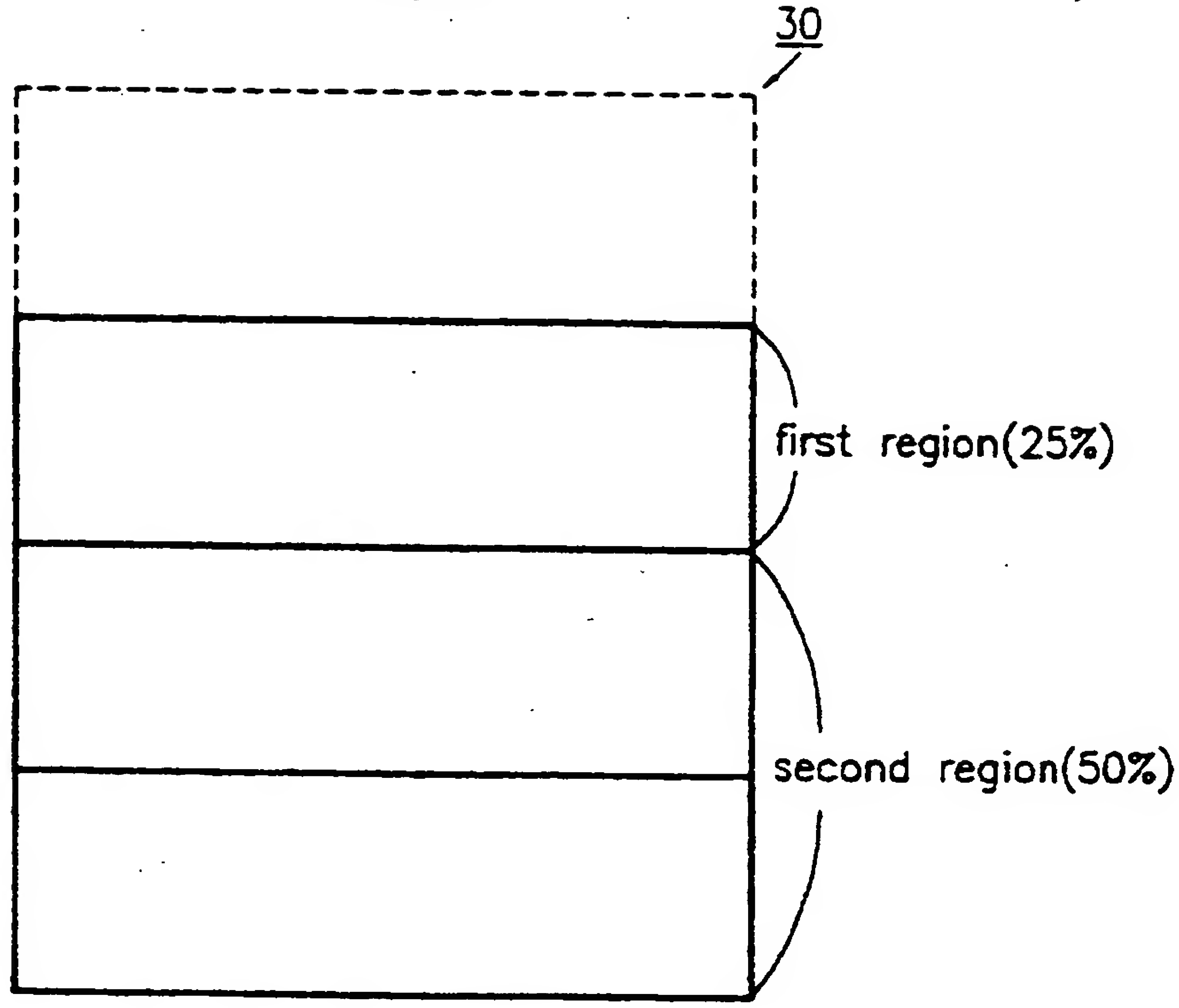


FIG.5

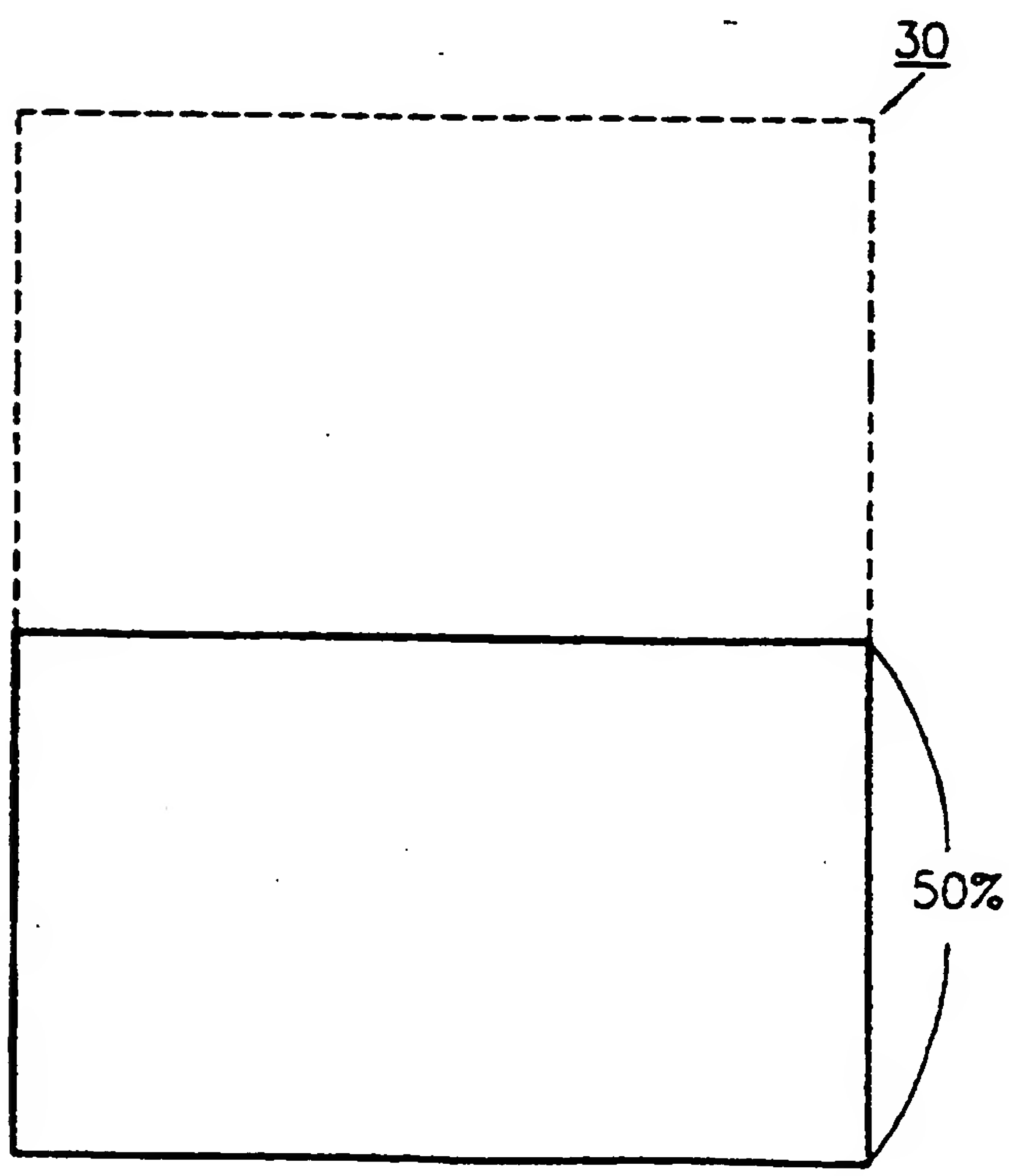


FIG.6

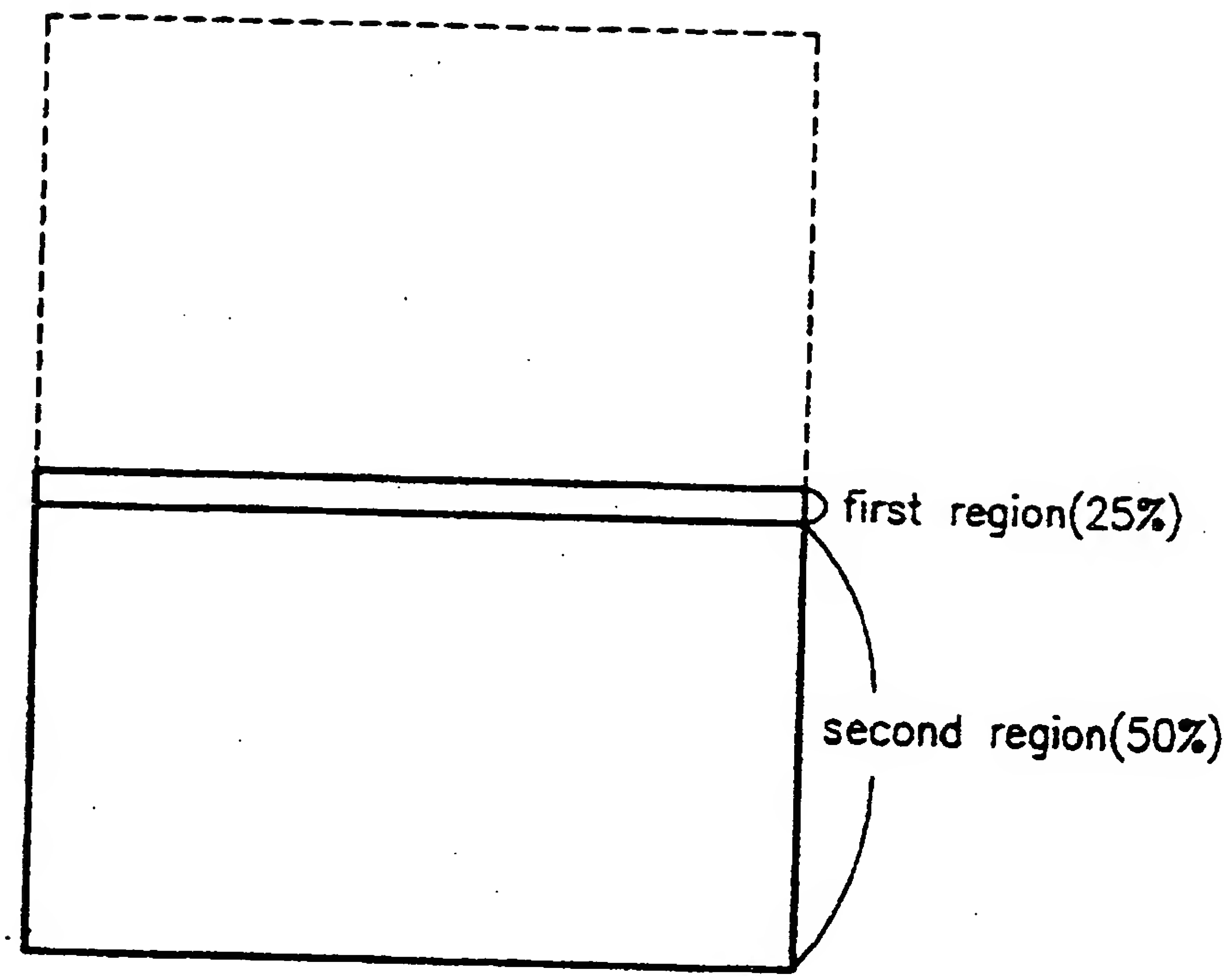
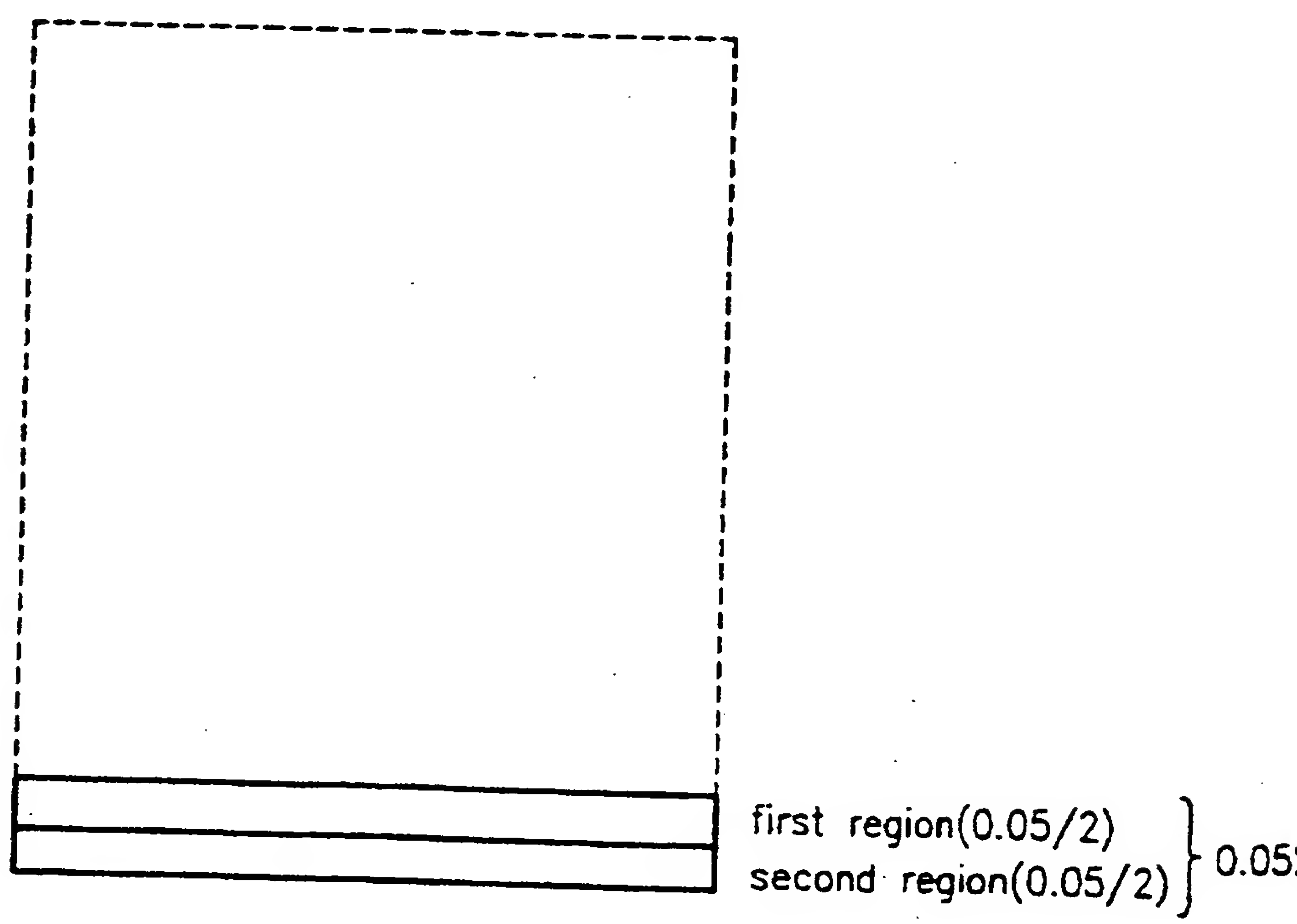

first region(25%)
second region(50%)

FIG.7


first region(0.05/2)
second region(0.05/2)
0.05

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METHOD FOR STORING VIDEO FRAME DATA IN A MEMORY

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method for storing video frame data in a memory of a video apparatus.

Discussion of Related Art

Generally, video frame data is made by a unit of a pixel and displayed on a screen by a unit of the pixel. For the effective transmission and storage, the video frame data is initially encoded. Since the video frame data is enormous in the amount of information, a video compression technique is used during encoding. The video compression is implemented by eliminating video information repeated between spatial and temporal domains or coding the video information to a constant form. As one of the most widely known video compression techniques, there is a MPEG (Moving Picture Expert Group) specification.

The MPEG specification initially encodes the video frame data by a unit of a macro block and decodes the encoded video

frame data by a unit of the macro block for the purpose of storage and display. Each macro block consists of 16 × 16 pixels, i.e. 16 scanning lines. The MPEG specification has recently been adopted for the high quality of an image in systems such as a digital TV, a DBS (direct broadcasting satellite), a DVD, and a HDTV (high definition television).

In an NTSC broadcasting system, one frame data includes 480 scanning lines each having 720 pixels, as shown in Fig. 1a. A moving picture is achieved by displaying about 30 frame data per second.

In a PAL broadcasting system, one frame data consists of 576 scanning lines each having 720 pixels, as shown in Fig. 1b. The moving picture is formed by displaying about 25 frame data per second.

Typically, one video data is divided into an odd field (or a top field) and an even field (or a bottom field), and displayed on the screen in order of the odd field and the even field. In the following description, the odd and even fields may be referred to as first and second fields without distinguishing them. Moreover, one video frame data is divided into a upper part and a lower part. In the NTSC system, the upper part and the lower part have 240 scanning lines respectively. Since the NTSC system uses an interlaced

scanning, one scanning line of the odd filed and one scanning line of the even field are alternatively displayed on the screen, as indicated in Fig. 2. Therefore, in the frame data of the NTSC system, the upper part and the lower part respectively have 120 scanning lines of the odd field and 120 scanning lines of the even field.

Fig. 3 is a schematic block diagram showing a typical decoding part of the video apparatus such as a television receiver and a video cassette recorder. A conventional method for storing the video frame data in a memory will now be described with reference to Fig. 3.

A decoder 20 sequentially decodes encoded video frame data by a control signal CS_1 of a controller 10. A memory 30 sequentially stores the video frame data generated from the decoder 20 by a unit of the frame data by another control signal CS_2 of the controller 10 and then supplies the stored frame data to another storage device 50 or a display unit 40, for example, a television receiver and a monitor. That is, each video frame data is supplied to the display unit 40 or the storage device 50 after it is completely stored in the memory 20.

In more detail, each video frame data consists of the odd field and the even field. The odd field data of the video

frame data generated from the decoder 20 is stored in a first region 30a of the memory 30, and the even field data thereof is stored in a second region 30b of the memory 30, as shown in Fig. 3b. In this case, each field data is sequentially stored in each region by a unit of a constant number of scanning lines, 8 or 16 scanning lines for example. Thus, if one frame data is divided into the odd field data and the even field data, and if these field data is stored in the first and second regions 30a and 30b, the memory 30 supplies the odd field data stored in the first region 30a to the storage device 50 or the display unit 40 by the control signal CS_2 of the controller 10 in stored order of 1a, 2a, 3a,...(n-1)a, na. Thereafter, the memory 30 supplies the even field data stored in the second region 30b to the display unit 40 or the storage device 50 in stored order of 1b, 2b, 3b,...(n-1)b, nb. The next video frame data generated from the decoder 20 is stored in the memory 30 in the same way as the above-described processes and then applied to the display unit 40 or the storage device 50.

It should be noted that each video frame data is supplied to the display unit to be displayed or to the another storage device to be stored after it is completely stored in the memory. Therefore, the memory 30 should have a capacity which

is capable of storing each video frame data to the maximum. However, there are disadvantages which will hereinafter be described. The memory is fabricated by a manufacturing company to a multiple of 2, that is, 1, 2, 4, 8 megabytes (MB), etc. Hence, the maximum capacity of the video frame data to be stored does not accurately coincide with the capacity of available memories. For example, in order to store the video frame data of the MPEG specification according to the PAL system, the memory capacity of a maximum of 1,866,240 bytes is needed. Further, in order to store each video bit stream before decoding, the memory capacity of 229,376 bytes is required. It is necessary to have the additional memory capacity of about 500,000 bytes in order to store on screen display (OSD) data, audio data and system data. Consequently, the memory capacity of about 2.6 MB is needed to store the video frame data of the MPEG specification according to the PAL system during decoding.

However, as previously noted, since the memory having the memory capacity of 2.6 MB is not fabricated, the memory having the capacity of 4 MB should be selected. Therefore, when designing the decoding part of the video apparatus, there occurs a unnecessary increase in manufacturing cost. Moreover, since the capacity of the video frame data for the PAL system

is larger than that for the NTSC system, the video frame data for the PAL system can not be stored in the memory corresponding to the NTSC system. In order words, the video apparatus of the PAL system is not compatible with that of the NTSC system.

SUMMARY OF THE INVENTION

Embodiments of the invention are directed to a method for storing video frame data in a memory that address one or more of the problems due to limitations and disadvantages of the related art.

It would be desirable to provide a method for storing video frame data in a memory which can reduce the capacity of a memory used in a decoding part of a video apparatus.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

The method for storing video frame data in a memory includes the steps of: sequentially receiving the video frame data; dividing each of the video frame data into a first part and a second part; storing the first part in the memory; and storing the second part in the memory while the stored first part is generated from the memory for one purpose, and generating the second part stored in the memory for the same purpose.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE ATTACHED DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the drawings. In the drawings:

Fig. 1a is a diagram showing the construction of one screen of an NTSC broadcasting system;

Fig. 1b is a diagram showing the construction of one screen of a PAL broadcasting system;

Fig. 2 is a diagram showing an interlaced scanning;

Fig. 3a is a block diagram showing a general decoding part of a video apparatus;

Fig. 3b is a diagram showing an example of how video frame data is stored in a frame memory according to the prior art;

Fig. 4 is a diagram showing one example that a frame memory which can store only 75% of video frame data is used in a decoding part according to a first embodiment of the present invention;

Fig. 5 is a diagram showing another example that a frame memory which can store only 50% of video frame data is used in a decoding part according to a second embodiment of the present invention;

Fig. 6 is a diagram showing still another example that a frame memory which can store only 52.5% of video frame data is used in a decoding part according to a third embodiment of the present invention; and

Fig. 7 is a diagram showing still yet another example that a frame memory which can store only 0.025% of video frame data is used in a decoding part according to a fourth

embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

One video frame data is divided into at least two parts, and each part is stored in a memory. While generating each part from the memory, the next part is stored in the memory. That is, while the previously stored part is generated from the memory, since the next part is stored in the memory, the capacity of the memory can be reduced.

A decoding part of a video apparatus for storing the video frame data in the memory is the same as Fig. 3. Therefore, the description thereof is omitted and constituents of Fig. 3 are referred to.

The capacity of the memory can be reduced to a desired degree depending on how one video frame data is divided and stored in the memory. To aid a understanding of this concept, a first example for dividing the video frame data into two parts before its storage, and a second example for dividing the video frame data into n parts will be

described. Actually, to divide the video frame data into n parts is to repeat the case that the video frame data is divided into two parts.

According to the first example, a method for storing the video frame data in the memory includes the steps of sequentially receiving the video frame data, dividing each frame data into a first part and a second part, storing the first part in the memory, and storing the second part in the memory while the stored first part is generated from the memory for one purpose and generating the second part stored in the memory for the same purpose.

The video frame data may be generated from the memory 30 by the controller 10 to be displayed through the display unit 40 such as a television set, or may be generated by the controller 10 to be stored in the storage device 50. In the above first example, a time to generate the first part from the memory 30 is the same as that to store the second part in the memory 30 because the second part is stored in the memory 30 while the first part is generated from the memory 30. Therefore, the memory 30 is a frame memory which can store one video frame data but its capacity is sufficient only if it can store half the video frame data. Further, it is favorable that the video frame data consists of a plurality of interlaced

scanning lines.

According to the second example, a method for storing the video frame data in the memory includes the steps of receiving the video frame data, dividing each frame data into n ($n \geq 2$) parts, storing a first part in the memory, storing a second part in the memory while the stored first part is generated from the memory for one purpose, storing other parts in the memory until an n-th part is stored in the memory while an (n-1)-th part is generated from the memory for the same purpose, and generating the stored n-th part for the same purpose.

In the second example, the memory may be the frame memory having the capacity which can store only 1/n of each video frame data. Each video frame data may be generated from the memory by the controller to be displayed or may be generated to be stored in another storage device.

Hereinafter, various embodiments of the present invention which can efficiently store one video frame data in the memory and thus reduce the capacity of the memory will be described.

In a first embodiment of the present invention, the memory having the capacity which can store only 75% of the video frame data is used in the decoding part of the video apparatus.

In Fig. 3b, it is assumed that the video bit stream

consists of upper and lower parts each having a first field (or a top field) and a second field (or a bottom field). The video bit stream is sequentially received through the decoder 20. The upper and lower parts of each video bit stream are sequentially decoded through the decoder 20.

As shown in FIG. 4, the controller 10 stores the first field (or the top field) of the decoded upper part in a first region (25% of the total memory capacity) of the memory 30, and stores the second field (or the bottom field) of the decoded upper part in a first part (25% of the total memory capacity) of a second region of the memory 30. The first field of the upper part stored in the first region of the memory 30 is generated to be displayed through the display unit or to be stored in another storage device. While the first field of the upper part is generated, the first field of the lower part is stored in the first region of the memory 30 and the second field of the lower part is stored in a second part (25% of the total memory capacity) of the second region of the memory 30. Thereafter, the controller 10 sequentially generates the first field of the lower part stored in the first region of the memory 30, and the second field of the upper part and the second field of the lower part stored in the second region to be displayed through the display unit 40 or to be stored in

the storage device 50.

As described above and as shown in Fig. 4, the frame memory which can store only 75% of the frame data corresponding to one image can be used in the decoding part of the video apparatus. In more detail, the first region of the frame memory 30 alternatively stores two top fields of one frame data, and therefore has the capacity which can store 25% of one frame data. The second region of the frame memory sequentially stores two bottom fields of one frame data and has the capacity which can store 50% of one frame data. That is, this embodiment is very useful in storing the video frame data of the MPEG specification in one frame memory having the small capacity. Therefore, it can be assumed that the video frame data is encoded by a unit of a macro block row, and thus the video frame data can be decoded by a unit of the macro block through the decoder 20. As is well known, the first and second fields are stored in the memory 30 and generated by a unit of a constant number of scanning lines. In the video frame data of the MPEG specification, since the video frame data is encoded and decoded by a unit of the macro block consisting of 16×16 pixels, the constant number can be easily adapted to one of 8 and 16.

The first and second fields stored in the frame memory 30

are generated to be displayed through the display unit or to be stored in another storage device. In the first embodiment of the present invention, although the first and second fields are defined as the top and bottom fields respectively, they may be defined as the bottom and top fields respectively. If so, the bottom field is stored in the memory 30 prior to the top field, and displayed through the display unit 40 or stored in the storage device 50. If a repeat field signal is supplied from the controller 10 or the exterior, the memory 30 may generate the second field once more in response to the repeat field signal. If the first field is defined as the top field, the bottom filed is generated once more, and if the first field is defined as the bottom field, the top field is generated once again.

If it is desired that the video data of the MPEG specification having 24 frame data per second is displayed to the NTSC system having 30 frame data per second, it is necessary to supply the repeat field signal to the memory 30 through the controller 10 in order to display an image decoded to the 24 frame data per second to the NTSC system of the 30 frame data per second. Then it is possible to display the 30 frame data per second. That is, if it is desired that the video signal of the 24 frame data per second is displayed to

the NTSC system of the 30 frame data per second, the first and second fields of one video frame data stored in the memory 30 are sequentially displayed. If the repeat field signal is supplied to the memory 30 before the next video frame data is displayed, the second filed of the video frame data is displayed once more, and then the first field of the next video frame data is displayed. Thereafter, the second field of the next video frame data is displayed. The first field is any one of the top and bottom fields and the second field is the other one thereof. Therefore, when the repeat field signal is supplied to the memory 30, the repeat field may be the top field or the bottom field. In the first embodiment of the present invention, since one video bit stream is divided into the upper and lower parts each consisting of the first and second fields, one video bit stream has 4 fields. However, if the repeat field signal is supplied and thus the 4 fields increases to 5 fields, the video data of the MPEG specification having the 24 frame data per second can be displayed to the 30 video frame data per second which is suitable for the NTSC system.

The video frame data (in particular, B data among intra-coded picture (I) data, predictive-coded (P) data and bidirectionally predictive-coded

(B) data) of the MPEG specification can be decoded and displayed irrespective of the NTSC and PAL systems. Generally, the capacity of the frame memory for storing the video frame data of the NTSC system is less than that for storing the video frame data of the PAL system by about 20%. In the case that the decoder 20 shown in Fig. 3a processes the video frame data of the PAL system while processing the video frame data of the NTSC system, since the capacity of the frame memory within a television receiver of the NTSC system is only 83% of the capacity of the video frame data of the PAL system, the capacity of the memory is absolutely insufficient. In order to make the compatible decoding part which is available in both the PAL and NTSC systems, the capacity of the frame memory should be adjusted to that of the PAL system. Then there is required the frame memory having the capacity of 4 MB which is greater than the memory capacity (2 MB) of the NTSC system. This problem is addressed by the above-mentioned memory storing method. That is, the video frame data of the NTSC system is stored in the frame memory of 2 MB which can store 100% of the video frame data and displayed on the screen. In the case that the decoder 20 receives and displays the video data of the MPEG specification of the PAL system, the frame memory of 2 MB used in the NTSC system can store only about 83% of the video

frame data of the PAL system. However, if the above-described storing method is applied, it is possible to decode and display the video frame data of the NTSC and PAL systems by use of the frame memory of only 2 MB without adding another frame memory.

A second embodiment of the present invention will now be described with reference to Fig. 3. In the second embodiment of the present invention, the memory having the capacity which can store only 50% of the video frame data is used in the decoding part of the video apparatus. It is assumed that the video bit stream consists of the first and second fields without being divided into the upper and lower parts.

The decoder 20 sequentially receives the video frame data consisting of the first and second fields. The decoder 20 decodes each frame data and stores only the first field among the decoded frame data in the frame memory 30 as shown in Fig. 5. The frame memory 30 generates the stored first field by the control of the controller 10. While the first field is generated, the decoder 20 again decodes the received video frame data by the controller 10 and stores only the second field among the again decoded frame data in the frame memory 30 by the controller 10. Finally, the memory 30 generates the stored second field.

As described in the first embodiment of the present invention, the first field may be any one of the top and bottom fields, and the second field may be the other one thereof. The second embodiment differs from the first embodiment in that the second embodiment requires the decoding twice. In order to display the video data of the MPEG specification having the 24 frame data per second to the NTSC system having the 30 frame data per second, the repeat field signal may be supplied to the frame memory 30 through the controller 10. The frame memory 30 generates the second field once more in response to the repeat field signal. The further generated second field may be the top field or the bottom field. The second embodiment can be used in both the video frame data of an interlaced system and the video frame data of a non-interlaced system, but it is not useful in the non-interlaced system since the decoding is unnecessarily performed twice.

The decoded first and second fields are generated from the frame memory 30 to be displayed on the display unit 40 such as a television set and a monitor or stored in the storage device 50. In the second embodiment, since the decoding is performed twice and the frame memory 30 stores only one field data during each decoding, the frame memory 30

has the capacity which can store only 50% of the video frame data. Therefore, the capacity of the frame memory used in the decoding part of the video apparatus can be reduced and can store the video frame data of other broadcasting systems having the larger amount of data by use of the frame memory used in the NTSC system of 2 MB.

As described above, this embodiment can be applied to the video data of the MPEG specification. In such a case, the video frame data is encoded by a unit of the macro block. The first and second fields are stored and generated by a unit of a constant number of scanning lines. The constant number of scanning lines may be 8 or 16 scanning lines since the video frame data of the MPEG specification is encoded and decoded by a unit of the macro block corresponding to 16 scanning lines of 16×16 pixels. The advantages of the second embodiment are the same as those of the first embodiment, and therefore no further description will be given.

A third embodiment of the present invention will now be described. In the third embodiment, the memory having the capacity which can store only 52.5% of the video frame data is used in the decoding part of the video apparatus.

The decoder 20 receives the video bit stream, i.e. the video frame data, consisting of the first and second fields.

The first and second fields are respectively divided into n parts, and the first and second fields divided into n parts are decoded. The first part to the n-th part of the decoded first field are sequentially stored in a first region (2.5%) of the frame memory 30 indicated in Fig. 6 and generated for one purpose. The first part to the n-th part of the decoded second fields are sequentially stored in a second region (50%) of the frame memory 30. Finally, each part of the second field stored in the second region of the frame memory 30 is generated in stored order.

The first field may be any one of the top and bottom fields and the second field may be the other one thereof. The video frame data according to the third embodiment of the present invention may be used in both the interlaced system and the non-interlaced system. The decoded first and second fields are generated to be displayed through the display unit 40 or to be stored in the storage device 50. The frame memory 30 can store and generate each decoded video frame data with the capacity which can store only 52.5% of one video frame data. The first and second regions of the frame memory 30 respectively occupy 2.5% and 50% out of 52.5% as shown in Fig. 6. In the video frame data of the MPEG specification, since the video frame data is encoded and decoded by a unit of the

macro block corresponding to 16 scanning lines, each 1/n of the first and second fields is equivalent to 8 scanning lines. After the first field divided into the n parts is generated from the frame memory 30, the second field stored in the frame memory 30 is generated in stored order by a unit of a constant number of scanning lines.

In more detail, the decoder 20 decodes the first part of the first field and the first part of the second field. The controller 10 stores the decoded first part of the first field in the first region (2.5%) of the fame memory 30 and stores the decoded first part of the second field in the second region (50%) of the memory frame 30. Thereafter, the controller 10 generates the first part of the first filed stored in the first region of the frame memory 30, and decodes the second part of the first field and the second part of the second field while the first part of the first field is generated. The controller 10 stores the decoded second part of the first field in the first region of the frame memory 30 and stores the decoded second part of the second field in the second region. The controller 10 repeats the decoding, storing and generating processes for other parts until the n-th part of the first field is generated and the n-th part of the second field is stored in the second region of the frame

memory 30. Finally, the first part to the n-th part of the second field stored in the second region of the frame memory 30 are sequentially generated in stored order. The second field can be generated once more by supplying the repeat field signal to the frame memory 30 through the controller 10.

Hereinafter, one example applied to B video data among the video frame data of the MPEG specification encoded by a unit of the macro block will be described.

The B video data may be contained in the NTSC system and may be contained in the PAL system. The B video data is one of 3 video data of the MPEG specification, that is, I (intra-coded Picture) data, P (predictive-coded) data and B (bidirectionally predictive-coded) data. If the decoder 20 decodes the video frame data, the controller 10 divides the decoded first and second fields into a unit of 8 scanning lines to be respectively stored in the first region (2.5%) and the second region (50%) of the frame memory 30. The decoded data of the B video data consists of a unit of the macro block (16 scanning lines) and the 16 scanning lines consist of the first field of 8 scanning lines stored in the first region of the frame memory 30 and the second field of 8 scanning lines stored in the second region of the frame memory 30. The first region (2.5%) of the frame memory 30 has the capacity which

can store the 16 scanning lines and the controller 10 stores the first field of the decoded 8 scanning lines in the first region. Thereafter, the controller 10 stores the decoded 8 scanning lines corresponding to the second field of the B video data in the second region (50%) of the frame memory 30.

The decoder 20 decodes the 16 scanning lines of a unit of the macro block row. The controller 10 stores the 8 scanning lines corresponding to the first field in an empty part of the first region (2.5%) of the frame memory 30 and stores the 8 scanning lines corresponding to the second field in the second region (50%) of the frame memory 30. At the same time, the 8 scanning lines of the first field stored in the first region are displayed. In the second region (50%) of the frame memory 30, the second field of the 16 scanning lines has been stored. Each time the 8 scanning lines are displayed, the macro block corresponding to the 16 scanning lines, that is, the first field of the 8 scanning lines and the second field of the 8 scanning lines are stored in the frame memory 30. Therefore, the decoding speed is twice the displaying speed. The advantages of the third embodiment are the same as those of the first and second embodiments.

A fourth embodiment of the present invention will now be described with reference to Fig. 3. In the fourth embodiment,

the memory having the capacity which can store only 0.025% of the video frame data is used in the decoding part of the video apparatus.

The decoder 20 receives the video frame data consisting of the first and second fields. The decoder 20 respectively divides the first and second fields into n parts, and decodes the first and second fields divided into the n parts. The controller 10 stores the decoded first field from the first part to the n-th part in the frame memory 30 and generates the stored first field for one purpose. The decoded second field is discarded. The decoder 20 decodes the first and second fields divided into the n parts once more. The first part to the n-th part of the decoded second field are sequentially stored in the frame memory 30 and generated for the same purpose. The decoded first field is discarded. As noted above, the first and second fields are sequentially displayed by decoding one video frame data twice. The decoding speed of the decoder 20 should be faster than twice the displaying speed of the display unit 40.

In more detail, assuming the video frame data is the B video data of the MPEG specification, the decoder 20 sequentially decodes the upper and lower parts of the video bit stream (the B video data of the MPEG specification) by a

unit of the macro block. The first field of 8 scanning lines of the decoded upper part is stored in a first region (0.025%/2) of the frame memory 30. The first field of the 8 scanning lines of the decoded lower part is stored in a second region (0.025%/2), and the first field of the upper part of the 8 scanning lines previously stored in the first region is displayed. That is, while displaying the 8 scanning lines of the first field of the upper part, the macro block (16 scanning lines) of the lower part is decoded. Only the first field of the lower part is stored in an empty part of the frame memory 30 and the second field of the lower part is discarded. If the first field of the decoded 8 scanning lines is again stored in the first region, the first field of the 8 scanning lines stored in the second region is displayed by the controller 10. The 8 scanning lines corresponding to the first field of the upper part are displayed after the 16 scanning lines corresponding to the macro block of the lower part are decoded. In such a manner, the first field is alternatively stored in the first and second regions of the frame memory 30 by a unit of the 8 scanning lines and displayed through the display unit 40. The decoding is performed once more during the next field time. Only the second field of the B video data is alternatively stored in the first and second regions of the

frame memory 30 and displayed through the display unit 40 by the controller 10. In this case, the data of the decoded first field is discarded.

Thus, one video frame data is decoded twice and a corresponding image is displayed. In the above description, the decoded first and second field are generated from the frame memory 30 to be displayed. However, the first and second fields may be generated to be stored in another storage.

As shown in Fig. 7, the frame memory 30 has the capacity which can store only 0.025% of one frame data. The frame memory 30 may have the capacity corresponding to 1/n of one frame data. Assuming that the video frame data has the MPEG specification, the frame data is encoded by a unit of the macro block. Therefore, the decoder should implement the decoding by a unit of the macro block. The above 1/n of first and second fields corresponds to the 8 scanning lines. The decoding speed should be faster than twice the displaying speed. Consequently, the decoder 20 decodes the first part of each field and stores only the first part of a corresponding field in the first region of the frame memory 30. Each second part of the first and second fields is decoded and the decoded second part of the corresponding field is stored in the second region of the frame memory 30. While the first part stored in

the first region is displayed through the display unit 40, the third part of each field is decoded and the third part of the corresponding field is stored in the first region. While the second part of the second region is displayed, the fourth part is decoded and stored in the second region. Other parts repeat the above processes until the n-th part of the corresponding field is generated from the frame memory 30. If the repeat field signal is supplied to the frame memory 30 by the controller 10, the video data of the MPEG specification having the 24 frame data per second can be displayed to the NTSC system having the 30 frame data per second.

As may be apparent from the aforementioned description, the capacity of the frame memory can be reduced by activating the utility of the frame memory. Furthermore, it is possible to decode the video frame data of the PAL system by use of the decoding device of the video frame data of the NTSC system. Therefore, an NTSC-only digital television receiver and a PAL-only digital television receiver can be simultaneously supported by one chip.

It will be apparent to those skilled in the art that various modifications and variations can be made in the method for storing video frame data in the memory of the present invention without departing from the scope of the

invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

CLAIMS

1. A method for storing video frame data in a memory, comprising the steps of:

sequentially receiving said video frame data;

dividing each of said video frame data into a first part and a second part;

storing said first part in said memory; and

storing said second part in said memory while the stored first part is generated from said memory for one purpose, and generating said second part stored in said memory for the same purpose.

2. A method for storing video frame data in a memory as set forth in claim 1, wherein said frame data is generated from said memory to be displayed.

3. A method for storing video frame data in a memory as set forth in claim 1, wherein said frame data is generated from said memory to be stored in another storage device.

4. A method for storing video frame data in a memory as set forth in claim 1, wherein a time to generate said first

part from said memory is the same as that to store said second part in said memory.

5. A method for storing video frame data in a memory as set forth in claim 1, wherein said memory is a frame memory.

6. A method for storing video frame data in a memory as set forth in claim 5, wherein said frame memory has a capacity which can not store all said frame data at the same time.

7. A method for storing video frame data in a memory as set forth in claim 1, wherein said frame data comprises a plurality of interlaced scanning lines.

8. A method for storing video frame data in a memory, comprising the steps of:

receiving said video frame data;

dividing the received frame data into n ($n \geq 2$) parts;

storing a first part in said memory;

storing a second part in said memory while the stored first part is generated from said memory for one purpose;

storing other parts in said memory until an n-th part is stored in said memory while an (n-1)-th part is generated from

said memory for the same purpose; and

generating the stored n-th part for the same purpose.

9. A method for storing video frame data in a memory as set forth in claim 8, wherein said memory is a frame memory which can store only 1/n of said video frame data.

10. A method for storing video frame data in a memory as set forth in claim 8, wherein said frame data is generated from said memory to be displayed.

11. A method for storing video frame data in a memory as set forth in claim 8, wherein said frame data is generated to be stored in another storage device.

12. A method for storing video frame data in a memory, comprising the steps of:

sequentially receiving said frame data consisting of upper and lower parts each including first and second fields;

sequentially decoding said upper and lower parts of each frame data;

storing the first and second fields of the decoded upper part in first and second regions of said memory, respectively;

generating the first field of said upper part stored in said first region of said memory for one purpose, storing the first field of said lower part in said first region while the first field of said upper part is generated, and storing the second field of said lower part in said second region of said memory; and

sequentially generating the first field of said lower part stored in said first region, the second field of said upper part stored in said second region, and the second field of said lower part stored in said second region.

13. A method for storing video frame data in a memory as set forth in claim 12, wherein said memory is a frame memory which can store only 75% of one frame data corresponding to one image.

14. A method for storing video frame data in a memory as set forth in claim 13, wherein said first region of said frame memory has a capacity which can store 25% of one frame data and wherein said second region of said frame memory has a capacity which can store 50% of one frame data.

15. A method for storing video frame data in a memory as

set forth in claim 12, wherein said frame data is encoded by a unit of a macro block suitable for a MPEG (Moving Picture Expert Group) specification, and therefore decoded by a unit of said macro block.

16. A method for storing video frame data in a memory as set forth in claim 12, wherein said first and second fields are stored and generated by a unit of a constant number of scanning lines.

17. A method for storing video frame data in a memory as set forth in claim 16, wherein said constant number of scanning lines is any one of 8 and 16 scanning lines.

18. A method for storing video frame data in a memory as set forth in claim 12, wherein said first and second fields stored in said memory are generated to be displayed.

19. A method for storing video frame data in a memory as set forth in claim 12, wherein said first and second fields stored in said memory are generated to be stored in another storage device.

20. A method for storing video frame data in a memory as set forth in claim 12, further comprising the step of generating the second field once more in response to a repeat field signal if said repeat field signal is supplied from the exterior.

21. A method for storing video frame data in a memory, comprising the steps of:

receiving said frame data consisting of first and second fields;

decoding said frame data, and storing only said first field among the decoded frame data in said memory;

generating said first field stored in said memory;

again decoding said frame data while said first field is generated, and storing only said second field among the again decoded frame data in said memory; and

generating said second field stored in said memory.

22. A method for storing video frame data in a memory as set forth in claim 21, further comprising the step of generating said second field once more in response to a repeat field signal if said repeat field signal is supplied from the exterior.

23. A method for storing video frame data in a memory as set forth in claim 21, wherein said frame data is suitable for an interlaced scanning system.

24. A method for storing video frame data in a memory as set forth in claim 21, wherein the decoded first and second fields are generated from said memory to be displayed.

25. A method for storing video frame data in a memory as set forth in claim 21, wherein the decoded first and second fields are generated from said memory to be stored in another memory device.

26. A method for storing video frame data in a memory as set forth in claim 21, wherein said memory has a capacity which can store only 50% of said frame data.

27. A method for storing video frame data in a memory as set forth in claim 21, wherein said frame data is encoded by a unit of a macro block.

28. A method for storing video frame data in a memory as set forth in claim 21, wherein said first and second fields

are stored in said memory and generated therefrom by a unit of a constant number of scanning lines.

29. A method for storing video frame data in a memory, comprising the steps of:

(a) receiving said frame data consisting of first and second fields;

(b) respectively dividing said first and second fields into n parts;

(c) decoding said first and second fields divided into the n parts;

(d) sequentially storing a first part to an n-th part of the decoded first field in a first region of said memory and generating each part of the stored first field for one purpose, and sequentially storing a first part to an n-th part of the decoded second field in a second region of said memory; and

(e) generating each part of the stored second field in stored order.

30. A method for storing video frame data in a memory as set forth in claim 29, wherein said video frame data is suitable for an interlaced scanning system.

31. A method for storing video frame data in a memory as set forth in claim 29, wherein said decoded first and second fields are generated from said memory to be displayed.

32. A method for storing video frame data in a memory as set forth in claim 29, wherein said decoded first and second fields are generated from said memory to be stored in another storage device.

33. A method for storing video frame data in a memory as set forth in claim 29, wherein said memory has a capacity which can store only 52.5% of said video frame data.

34. A method for storing video frame data in a memory as set forth in claim 33, wherein said first region of said memory occupies 2.5% out of 52.5% and wherein said second region of said memory occupies 50% out of 52.5%.

35. A method for storing video frame data in a memory as set forth in claim 29, wherein each 1/n of said first and second fields corresponds to 8 scanning lines.

36. A method for storing video frame data in a memory as

set forth in claim 29, wherein said step (d) comprises the steps of:

decoding respective first parts of said first and second fields, storing the decoded respective first parts of said first and second fields in first and second regions of said memory respectively;

decoding respective second parts of said first and second fields while the stored first part of said first field is generated, and storing the decoded respective second parts of said first and second fields in said first and second regions of said memory respectively;

repeating the decoding and storing steps for other parts of said first and second fields until an n-th part of said first field is generated from said memory and an n-th part of said second field is stored in said second region of said memory; and

sequentially generating the first part to the n-th part of said second field stored in said second region of said memory.

37. A method for storing video frame data in a memory, comprising the steps of:

(a) receiving said frame data consisting of first and

second fields;

(b) respectively dividing said first and second fields into n parts;

(c) decoding said first and second fields divided into the n parts, sequentially storing a first part to an n-th part of the decoded first field in said memory, and generating each part of the stored first field for one purpose; and

(d) again decoding said first and second fields divided into the n parts, sequentially storing a first part to an n-th part of the decoded second field in said memory, and generating each part of the stored second field for the same purpose.

38. A method for storing video frame data in a memory as set forth in claim 37, wherein said video frame data is suitable for an interlaced scanning system.

39. A method for storing video frame data in a memory as set forth in claim 37, wherein said decoded first and second fields are generated from said memory to be displayed.

40. A method for storing video frame data in a memory as set forth in claim 37, wherein said decoded first and second fields are generated from said memory to be stored in another

storage device.

41. A method for storing video frame data in a memory as set forth in claim 37, wherein said memory has a capacity which can store only 0.025% of said video frame data.

42. A method for storing video frame data in a memory as set forth in claim 37, wherein said memory has a capacity corresponding to 1/n of said video frame data.

43. A method for storing video frame data in a memory as set forth in claim 37, wherein said video frame data is encoded by a unit of a macro block and therefore decoded by a unit of the macro block.

44. A method for storing video frame data in a memory as set forth in claim 37, wherein each 1/n of said first and second fields corresponds to 8 scanning lines.

45. A method for storing video frame data in a memory as set forth in claim 37, wherein said steps (c) and (d) respectively comprise the steps of:

decoding respective first parts of said first and second

fields, and storing the decoded first part of a corresponding field in a first region of said memory;

decoding respective second parts of said first and second fields, and storing the decoded second part of the corresponding field in a second region of said memory;

decoding respective third parts of said first and second fields while the first part stored in said first region of said memory is generated from said memory, and storing the decoded third part of the corresponding field in said first region of said memory;

decoding respective fourth parts of said first and second fields while the second part stored in said second region of said memory is generated, and storing the decoded fourth part of the corresponding field in said second region of said memory; and

repeating the decoding and storing steps for other parts of said first and second fields until an n-th part of the corresponding field is generated from any one of said first and second regions of said memory.

46. A method for storing video frame data in a memory substantially as herein described with reference to Figures 4 to 7 of the accompanying drawings.

The Patent Office

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Application No: GB 9707807.5
Claims searched: 1 to 28

Examiner: John Donaldson
Date of search: 12 June 1997

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Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H4F(FKA, FKE, FKX, FRC, FRD, FRG, FRM, FRP, FRR, FRT, FRW, FRX)

Int Cl (Ed.6): H04N 5/00, 5/76, 5/78, 5/781, 5/782, 5/783, 5/903, 5/907, 5/91, 5/915, 5/917, 5/919, 5/93, 5/937, 7/00, 7/01, 7/24, 7/26, 7/32, 7/34, 7/36, 7/48, 7/50, 9/00, 9/79, 9/797, 9/87, 9/877, 11/00, 11/02, 11/04

Other: Online:WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 2182817 A	(SONY), see page 3, lines 28 to 119	1 to 5, 7, 8, 10, 11, 21, 23 to 25, 28
X	EP 0621730 A2	(GENERAL INSTRUMENT), see column 7, line 9 to column 8, line 2	1 to 5, 7, 8, 10, 11, 21, 23 to 25, 28
X	EP 0618722 A1	(LABORATOIRES D'ELECTRONIQUE PHILIPS), see US 5561465 below	1 to 8, 10, 11, 21 to 25, 27, 28
&, X, P	US 5561465	(FAUTIER), see column 4, line 18 to column 6, line 7	1 to 8, 10, 11, 21 to 25, 27, 28
X	US 4847809	(SUZUKI), see abstract	1 to 5, 7, 8, 10, 11, 21, 23 to 25, 28

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
		E	Patent document published on or after, but with priority date earlier than, the filing date of this application.
&	Member of the same patent family		

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Application No: GB 9707807.5
Claims searched: 1 to 28

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Category	Identity of document and relevant passage	Relevant to claims
X	US 4823302 (CHRISTOPHER), see column 3, line 38 to column 4, line 64	1 to 5, 7, 8, 10, 11, 21, 23 to 25, 28

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
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